General Description

The AAT4674/4674-1 are members of Analogic-Tech's Application Specific Power Management SmartSwitch™ family. These devices are dual input single output power supply selector switches designed to operate from batteries, or any other power supply with an input voltage up to 6V.

The AAT4674/4674-1 connects the supply voltage on IN1 to OUT, or IN2 to OUT, through a very low $R_{DS(ON)}$ power MOSFET that minimizes voltage drops and power dissipation. The enable (EN) and select (SEL) pin voltages control the operational state of the internal power MOSFET switches. Once enabled, the SEL pin will switch between the IN1 and IN2 inputs. If both input voltages are below the UVLO, then the AAT4674 output floats. In the case of the AAT4674-1, if one of the input voltages is above the UVLO threshold then that input voltage that is above the UVLO threshold is passed through to the output.

The two power switches are current limited and the current limit thresholds can be programmed through the resistors on IIN1 and IIN2 pins respectively.

The AAT4674/4674-1 are available in thermally enhanced, space-saving Pb-free 12-pin TSOPJW packages. The AAT4674/4674-1 are specified for operation over the -40°C to +85°C temperature range.

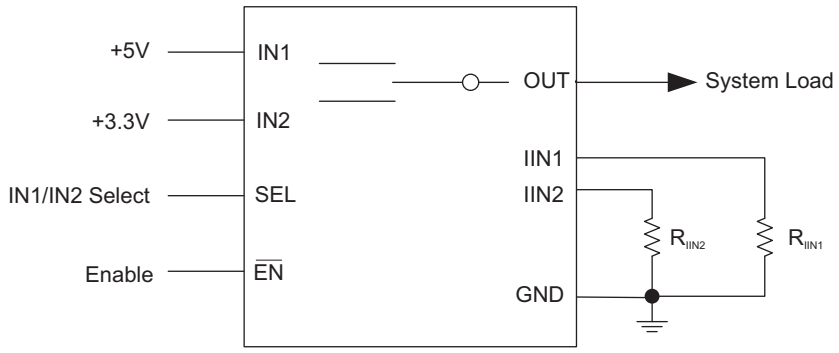
Features

- Input Voltage Supply Range: 2.5V to 6V
- High Level of Integration:
  - — Reverse Blocking Diode
  - — Current Sensing
  - — Programmable Current Limit
  - — Single Control Pin Switching
- Break-Before-Make Switch-Over
  - — Minimum Output Voltage Drop During Change-Over
- Shutdown Current < 1µA
- Thermal Protection
- TSOPJW-12 Package

Applications

- Bluetooth™ Headsets
- Cell Phones
- Digital Still Cameras
- MP3 Players
- Personal Data Assistants (PDAs)
- Set Top Boxes

Typical Application

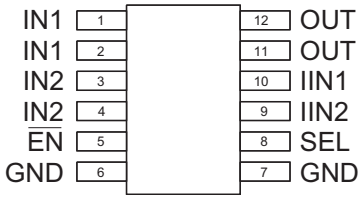


Pin Descriptions

Pin Number	Name	Type	Function
1, 2	IN1	I	Power supply 1 input.
3, 4	IN2	I	Power supply 2 input.
5	$\overline{EN}$		Enable pin, active low.
6, 7	GND	I/O	Ground.
8	SEL	I	IN2 or IN1 select input. Logic '0' → OUT = IN1 Logic '1' → OUT = IN2
9	IIN2	I	IN2-OUT switch current limit set resistor input.
10	IIN1	I	IN1-OUT switch current limit set resistor input.
11, 12	OUT	O	Output pin.

Pin Configuration

TSOPJW-12
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{INX}	[IN1, IN2] to GND	-0.3 to 6.5	V
V_N	[OUT, $\overline{EN}$, IIN1, IIN2, SEL] to GND	-0.3 to V_{INX} + 0.3	V
T_{LEAD}	Maximum Soldering Temperature (at Leads)	300	°C
I_{OUT}	Maximum Output Current	3	A

Thermal Information[2]

Symbol	Description	Value	Units
θ_{JA}	Maximum Thermal Resistance	160	°C/W
P_D	Maximum Power Dissipation	625	mW
T_J	Operating Junction Temperature Range	-40 to 150	°C

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on a FR4 board.

Electrical Characteristics[1]

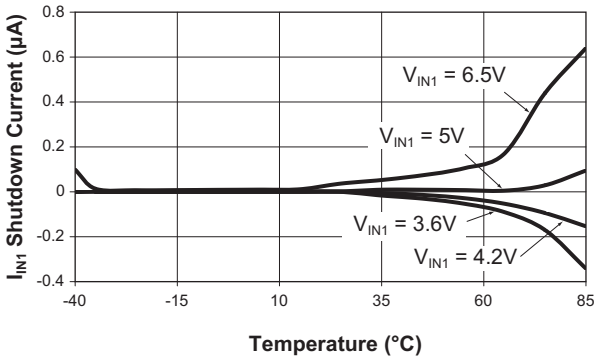
V_{INX} = 5V, T_A = -40 to +85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Operation						
V_{IN1}	IN1 Operating Voltage Range		2.5		6	V
V_{IN2}	IN2 Operating Voltage Range		2.5		6	V
V_{UVLO_IN1}	IN1 Under-Voltage Lockout	Rising edge			2.3	V
		Hysteresis		0.1		
V_{UVLO_IN2}	IN2 Under-Voltage Lockout	Rising edge			2.3	V
		Hysteresis		0.1		
I_{IN1_OP}	IN1 Normal Operating Current	V_{IN1} = 5V, $V_{\overline{EN}}$ = 0V		10	30	µA
I_{IN1_SHDN}	IN1 Shutdown Mode Current	V_{IN1} = $V_{\overline{EN}}$ = 5V, OUT open			1	µA
I_{IN1_SLP}	IN1 Sleep Current	V_{IN1} = 2.5V, V_{IN2} = 5V, $V_{\overline{EN}}$ =0V		1	5	µA
I_{IN2_OP}	IN2 Normal Operating Current	V_{IN2} = 5V, $V_{\overline{EN}}$ = 0V		10	30	µA
I_{IN2_SHDN}	IN2 Shutdown Mode Current	V_{IN2} = $V_{\overline{EN}}$ = 5V, OUT open			1	µA
I_{IN2_SLP}	IN2 Sleep Current	V_{IN1} = 5V, V_{IN2} = 2.5V, $V_{\overline{EN}}$ = 0V		1	5	µA
Power Switches						
$R_{DS(ON)\ IN1}$	IN1-to-OUT FET On-Resistance	V_{IN1} = 5.0V		0.12	0.15	Ω
		V_{IN1} = 3.5V		0.14	0.18	
$R_{DS(ON)\ IN2}$	IN2-to-OUT FET On-Resistance	V_{IN2} = 5.0V		0.12	0.15	Ω
		V_{IN2} = 3.5V		0.14	0.18	
V_{DROOP_OUT}	OUT Voltage Droop From the Lower Voltage of IN1 and IN2, When Switching Over Between IN1 and IN2	$I_{O(OUT)}$ = 0.5A, $C_{O(OUT)}$ = 10µF		150		mV
Current Regulation						
t_{SOFT_START}	Soft-Start Delay	Delay of start from $\overline{EN}$, or UVLO		100		µs
I_{LIM_range}	IN1/IN2 Current Limit Range		0.2		2.0	A
I_{LIM_ACC}	IN1/IN2 Current Limit Accuracy	$R_{IIN1/IIN2}$ = 100kΩ	0.8	1	1.2	A
Logic Control / Protection						
$V_{IH(\overline{EN})}$	Logic High Threshold		1.6			V
$V_{IL(\overline{EN})}$	Logic Low Threshold				0.4	V
T_{SHDN}	Chip Thermal Shutdown Temperature	Threshold		140		°C
		Hysteresis		15		

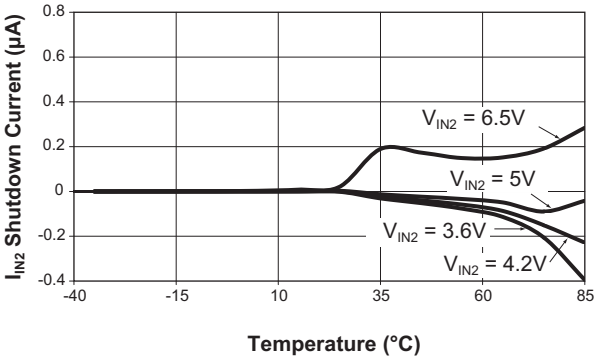
1. The AAT4674 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.

Typical Characteristics

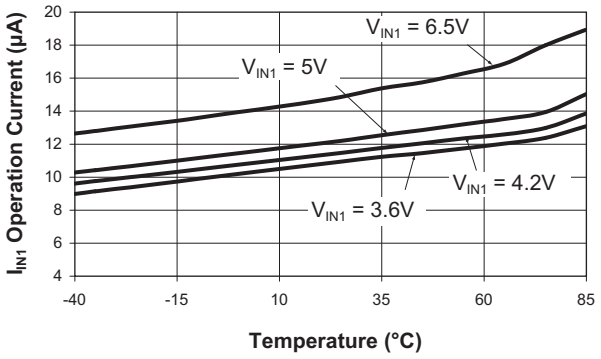
I_{IN1} Shutdown Current vs. Temperature



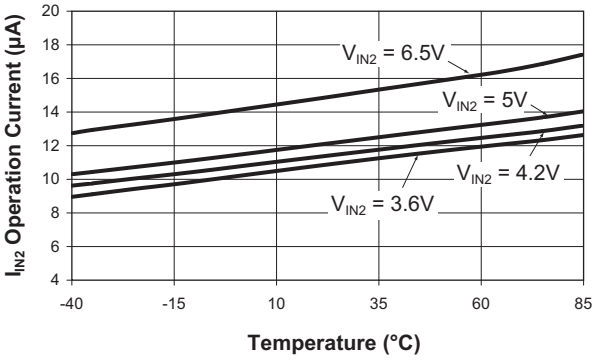
I_{IN2} Shutdown Current vs. Temperature



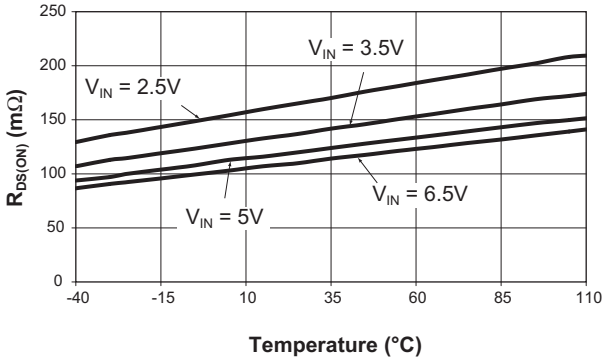
I_{IN1} Operation Current vs. Temperature
(I_{OUT} = 0A)



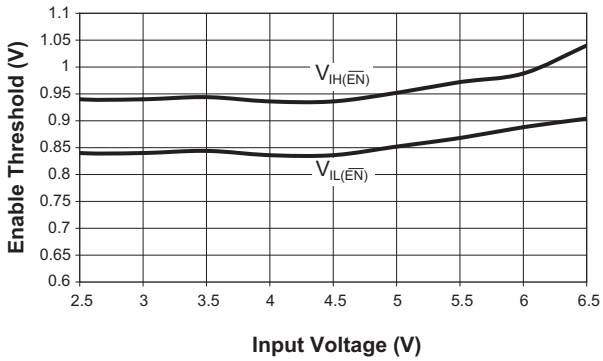
I_{IN2} Operation Current vs. Temperature
(I_{OUT} = 0A)



$R_{DS(ON)}$ vs. Temperature

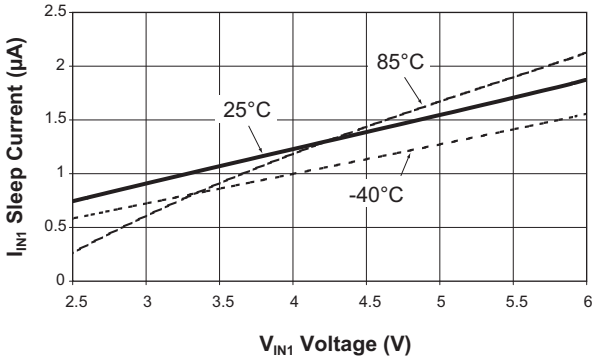


Enable Threshold vs. Input Voltage

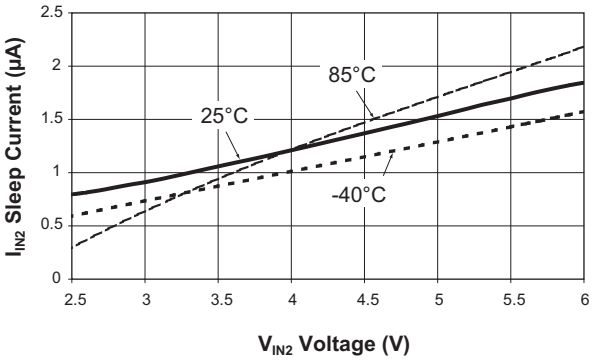


Typical Characteristics

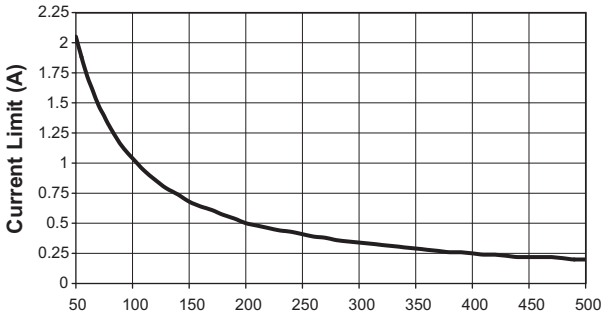
I_{IN1} Sleep Current vs. V_{IN1} Voltage
(V_{IN2} = 6.5V)



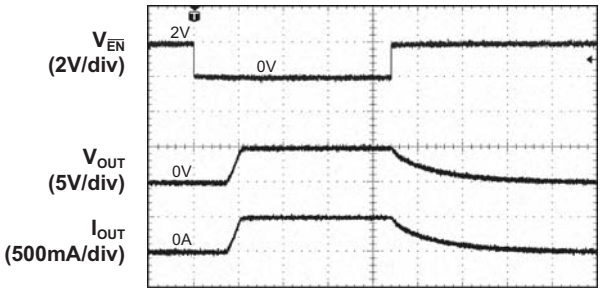
I_{IN2} Sleep Current vs. V_{IN2} Voltage
(V_{IN1} = 6.5V)



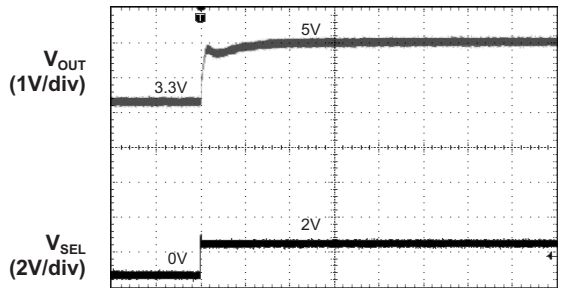
Current Limit vs. $R_{IIN1/IIN2}$
(V_{IN1} = 5V; V_{IN2} = 3.3V; V_{OUT} = V_{IN2} or V_{OUT} = V_{IN1})



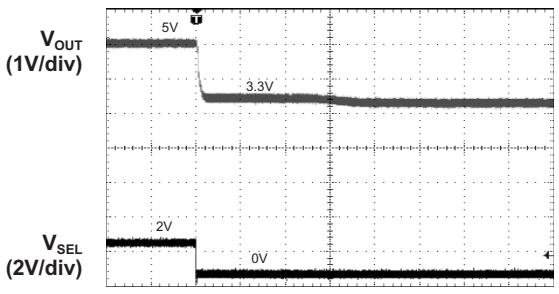
Turn-On/Off Response
(R_{OUT} = 10Ω; V_{IN} = 5V)



3.3V to 5V Transition Response
(I_{OUT} = 500mA, C_{OUT} = 10µF)

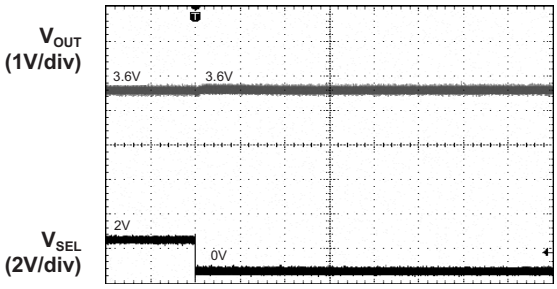


5V to 3.3V Transition Response
(I_{OUT} = 500mA, C_{OUT} = 10µF)



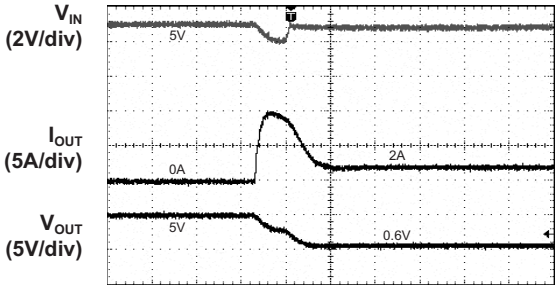
Typical Characteristics

3.6V to 3.6V Transition Response
(I_{OUT} = 500mA, C_{OUT} = 10µF)



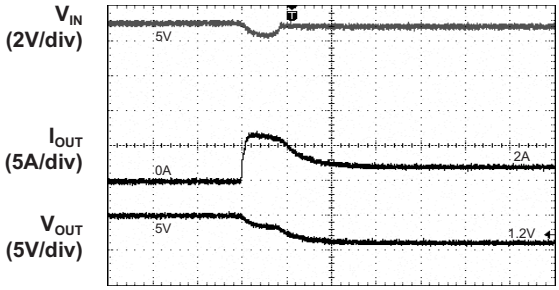
Time (40µs/div)

Short Circuit Through 0.3Ω Response



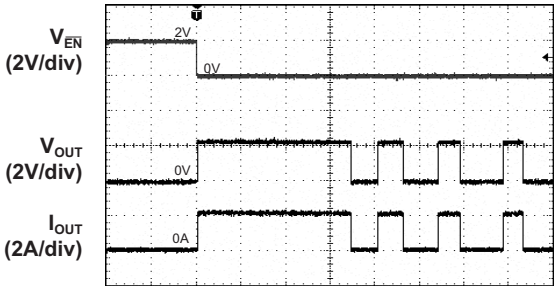
Time (10µs/div)

Short Circuit Through 0.6Ω Response



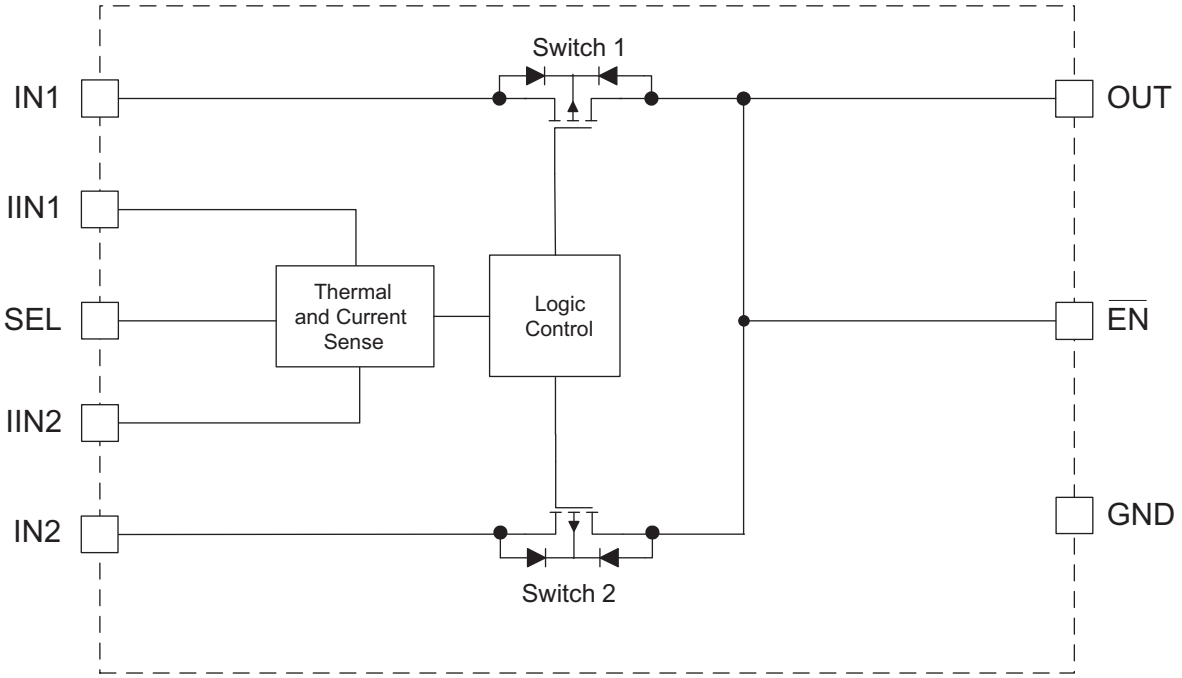
Time (10µs/div)

Thermal Shutdown Response
(V_{IN} = 5V)



Time (40ms/div)

Functional Block Diagram



Truth Table

Input Conditions			AAT4674	AAT4674-1
V_{IN1} > UVLO	V_{IN2} > UVLO	SEL	V_{OUT}	V_{OUT}
N	N	X	Floating	Floating
Y	N	X	Floating	V_{IN1}
N	Y	X	Floating	V_{IN2}
Y	Y	0	V_{IN1}	V_{IN1}
Y	Y	1	V_{IN2}	V_{IN2}

Y = Yes, N = No, X = don't care.

Functional Description

To power the output, both input supplies (IN1 and IN2) must be above the UVLO threshold. If either supply input is below the UVLO threshold then the output will float or, in the case of the AAT4674-1 the output will be the input supply that is above the UVLO threshold. If both supplies are above the UVLO threshold and the device is enabled, the AAT4674/AAT4674-1 will connect the supply from IN1 to OUT when the SEL pin is LOW (logic '0'), and when the SEL pin is HIGH (logic '1') then the supply on IN2 is connected to the OUT pin. Consult the above "Truth Table" for the summarized AA4674/4674-1 operational details.

The two internal power switches are current limited and the limiting thresholds can be programmed through the resistors on the IIN1 and IIN2 pins respectively.

Applications Information

Input Capacitors

A 1µF or greater capacitor is generally recommended between IN1 and GND (C_{IN1}), and between IN2 and GND (C_{IN2}). An input capacitor is not required for basic operation; however, it is useful in preventing load transients from affecting upstream circuits. Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN1}/C_{IN2}. There is no specific capacitor equivalent series resistance (ESR) requirement for C_{IN1}/C_{IN2}. However, for higher current operation, ceramic capacitors are recommended for C_{IN1}/C_{IN2} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

A 1µF or greater capacitor is required between OUT and GND (C_{OUT}). As with the input capacitor, there is no specific capacitor ESR requirement. If desired, C_{OUT} may be increased to accommodate any load transient condition.

$\overline{EN}$ Input

The AAT4674/4674-1 is enabled when $V_{\overline{EN}}$ is ≤ 0.4V (logic '0'), conversely the AAT4674/4674-1 is disabled when $V_{\overline{EN}}$ is ≥ 1.6V (logic '1').

SEL Input

When V_{SEL} is ≤ 0.4V (logic '0') the output voltage equals power supply 1 input ($V_{OUT} = V_{IN1}$), and conversely when V_{SEL} is ≥ 1.6V (logic '1') the output voltage equals power supply 2 input ($V_{OUT} = V_{IN2}$).

Current Limit Resistor Selection

The current limits for power supply 1 and power supply 2 inputs are set by resistors connected between IIN1/IIN2 and GND. The following equation can be used to select the appropriate resistor for a particular current limit:

$$I_{CLINX} = \left(\frac{V_{IINX}}{R_{IINX}}\right) \cdot 200k$$

I_{CLINX}	Current limit for IN1 and/or IN2 pins respectively
V_{IINX}	Internally Regulated Voltage [0.5V ± 20%] on the IIN1 and IIN2 pins respectively
R_{IINX}	IIN1 and/or IIN2 Resistor
200k	Internal Gain Factor

Design Example

A particular application requires that the current limit for IN1 be set to 2A and the current limit for IN2 be set to 0.2A. What value of resistor is required for the IIN1 and IIN2 pins respectively?

For IN1 (power supply 1 input):

$$R_{IIN1} = \left(\frac{V_{IIN1}}{I_{CLIN1}}\right) \cdot 200k$$

$$= \left(\frac{0.5V}{2A}\right) \cdot 200k$$

$$= 50k\Omega \text{ (49.9k}\Omega \text{ standard value)}$$

For IN2 (power supply 2 input):

$$R_{IIN2} = \left(\frac{V_{IIN2}}{I_{CLIN2}}\right) \cdot 200k$$

$$= \left(\frac{0.5V}{0.2A}\right) \cdot 200k$$

$$= 500k\Omega \text{ (499.9k}\Omega \text{ standard value)}$$

Thermal Considerations

Since the AAT4674/4674-1 have an internal current limit and over-temperature protection (thermal shutdown), junction temperature is rarely a concern. However, if the application requires large currents in a high temperature environment, it is possible that temperature rather than current limit will be the dominant regulating condition. In these applications, the maximum current available without risk of an over-temperature condition must be calculated. The maximum internal temperature while current limit is not active can be calculated using Equation 1 (Eq. 1).

Eq. 1: $T_{J(MAX)} = I_{MAX}^2 \cdot R_{DS(ON)(MAX)} \cdot R_{\theta JA} + T_{A(MAX)}$

In Equation 1, I_{MAX} is the maximum current required by the load. $R_{DS(ON)(MAX)}$ is the maximum rated $R_{DS(ON)}$ of the AAT4674/4674-1 at high temperatures (consult the "R_{DSON} vs. Temperature" performance graph in the "Typical Characteristics" section of this datasheet). For estimating the $R_{DS(ON)(MAX)}$ use the data on the "R_{DSON} vs Temperature" performance graph and increase the value from the performance graph by 50%. $R_{\theta JA}$ is the thermal resistance between the AAT4674/4674-1 and the printed circuit board (PCB) onto which it is mounted; $R_{\theta JA}$ is the thermal resistance of the TSOPJW-12 package. $T_{A(MAX)}$ is the maximum ambient temperature that the PCB under the AAT4674/4674-1 would be if the AAT4674/4674-1 were not dissipating power. Equation 1 can be rearranged to solve for I_{MAX}, into Equation 2 (Eq. 2).

Eq. 2: $$I_{MAX} = \sqrt{\frac{T_{SD(MIN)} - T_{A(MAX)}}{R_{DS(ON)(MAX)} \cdot R_{\theta JA}}}$$

$T_{SD(MIN)}$ is the minimum temperature required to activate the AAT4674/4674-1 over-temperature protection (thermal shutdown). With typical specification of 140°C, 125°C is a safe minimum value to use.

For example, for a 2.5V input power supply application that is specified to operate in 50°C environments where the PCB operates at temperatures as high as 85°C. The application is sealed and its PCB is small, causing $R_{\theta JA}$ to be approximately 160°C/W. The $R_{DS(ON)(MAX)}$ is estimate to be 300mΩ (from the "$R_{DS(ON)}$ vs. Temperature" performance graph, where V_{IN} = 2.5V at 85°C plus 50%). To find the maximum current (I_{MAX}) for this application use Equation 2:

$$I_{MAX} = \sqrt{\frac{125°C - 85°C}{300m\Omega \cdot 160°C/W}} = 0.913A$$

PCB Layout Recommendations

For proper thermal management, to minimize PCB trace resistance, and to take advantage of the low $R_{DS(ON)}$ values of the two internal power switches in the AAT4674/4674-1, certain circuit board layout rules should be followed: IN1, IN2, and OUT should be routed using wider than normal traces. The two IN1 pins (1 and 2) and two IN2 pins (3 and 4) should be connected to the same wide PCB trace; and GND should be connected to a ground plane. For best performance, the input capacitors (C_{IN1}/C_{IN2}) and output capacitors (C_{OUT}) should be placed as close to the package pins as possible. The AAT4674/4674-1 evaluation board layout follows the printed circuit board layout recommendations and can be used as an example of an optimal board layout.

Evaluation Board Schematic

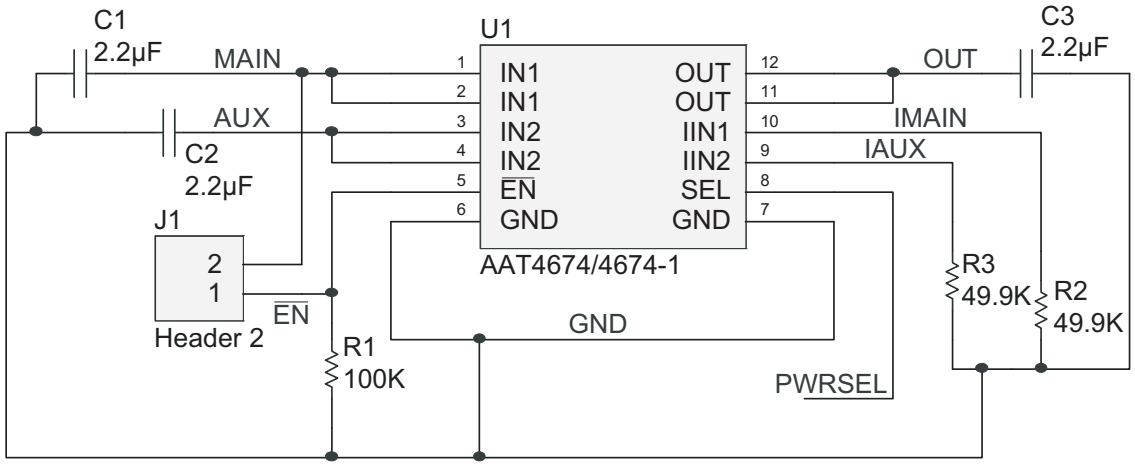


Figure 1: AAT4674/AAT4674-1 Evaluation Board Schematic.

Evaluation Board Layout

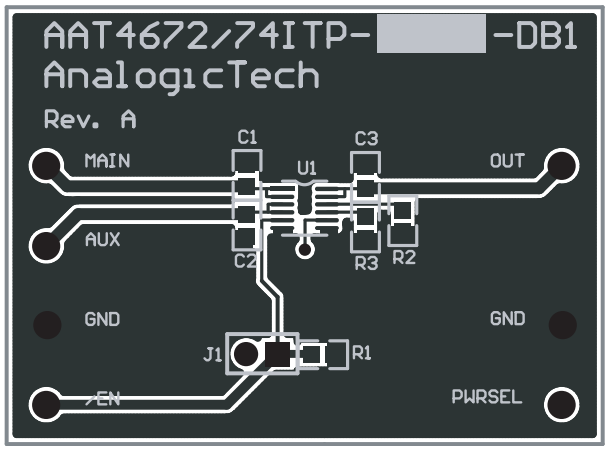


Figure 2: AAT4674/AAT4674-1 Evaluation Board Top Side Layout.

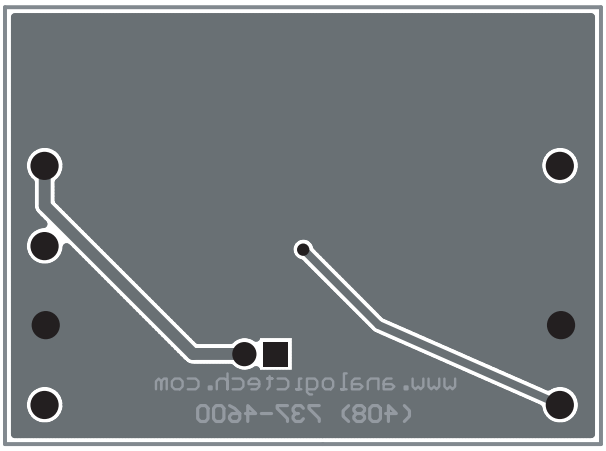


Figure 3: AAT4674/AAT4674-1 Evaluation Board Bottom Side Layout.

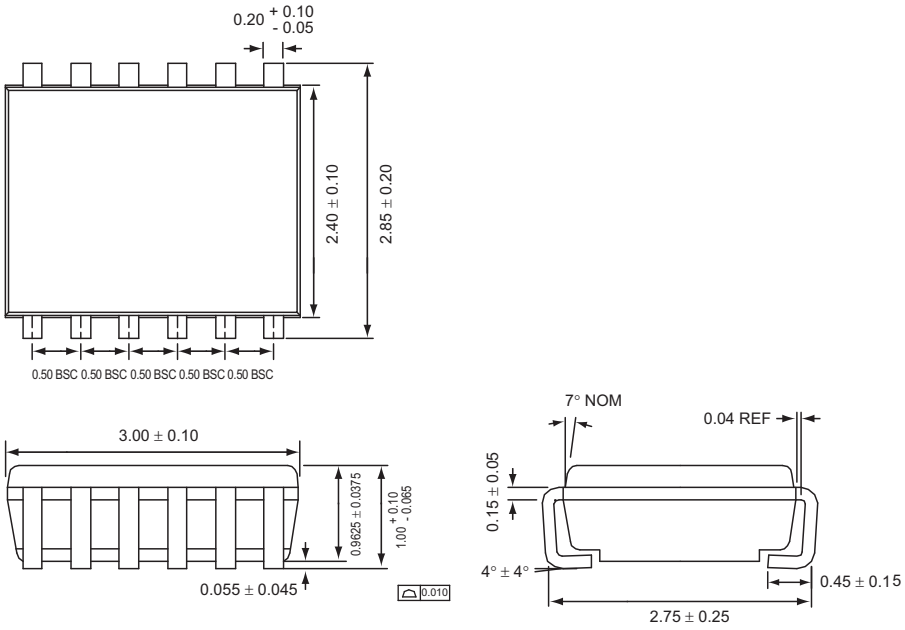
Ordering Information

Package	Marking[1]	Part Number (Tape and Reel)[2]
TSOPJW-12	ZVXYY	AAT4674ITP-T1
TSOPJW-12	YTXYY	**AAT4674ITP-1-T1**

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/pbfree.

Package Information

TSOPJW-12



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

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